

Micropower Precision Triple Supply Monitor

June 1998

FEATURES

- Simultaneously Monitors 2.5V, 3.3V and Adjustable Inputs
- Guaranteed Threshold Accuracy: $\pm 0.75\%$
- Low Supply Current: 20 μ A
- Internal Reset Time Delay: 200ms
- Manual Pushbutton Reset Input
- Active Low and Active High Reset Outputs
- Active Low "Soft" Reset Output
- Power Supply Glitch Immunity
- Guaranteed $\overline{\text{RESET}}$ for $V_{CC3} \geq 1\text{V}$ or $V_{CC25} \geq 1\text{V}$
- 8-Pin SO and MSOP Packages

APPLICATIONS

- Desktop Computers
- Notebook Computers
- Intelligent Instruments
- Portable Battery-Powered Equipment


DESCRIPTION

The LTC[®]1326-2.5 is a triple supply monitor intended for systems with multiple supply voltages. It provides micro-power operation, small size and high accuracy supply monitoring.

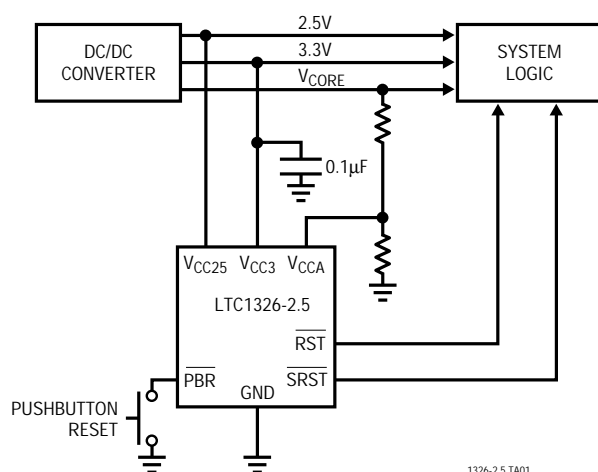
Tight 0.75% threshold accuracy and glitch immunity ensure reliable reset operation without false triggering. The 20 μ A typical supply current makes the LTC1326-2.5 ideal for power-conscious systems.

The $\overline{\text{RST}}$ output is guaranteed to be in the correct state for V_{CC25} or V_{CC3} down to 1V. The LTC1326-2.5 may also be configured as a dual or single supply monitor. Allowed configurations are 3.3V and 2.5V, 3.3V and Adj, or 3.3V only.

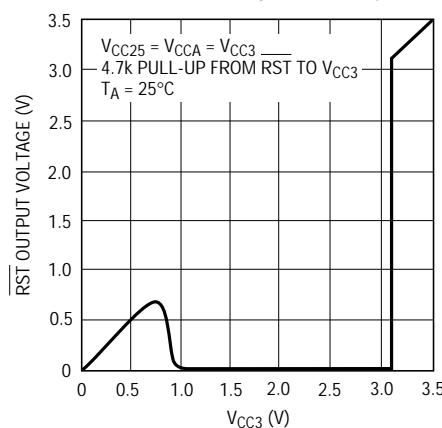
A manual pushbutton reset input provides the ability to generate a very narrow "soft" reset pulse (100 μ s typ) or a 200ms reset pulse equivalent to a power-on reset. Both $\overline{\text{SRST}}$ and $\overline{\text{RST}}$ outputs are open-drain and can be OR-tied with other reset sources.

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TYPICAL APPLICATION



$\overline{\text{RST}}$ Output Voltage vs Supply Voltage



1326-2.5 TA02

LTC1326-2.5

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Terminal Voltage

| | |
|--------------------------------------|-------------------------------|
| V_{CC3} , V_{CC25} , V_{CCA} | –0.5V to 7V |
| \overline{RST} , \overline{SRST} | –0.5V to 7V |
| \overline{RST} | –0.5V to ($V_{CC3} + 0.3V$) |
| \overline{PBR} | –7V to 7V |

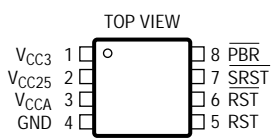
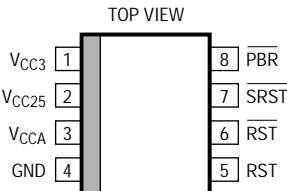
Operating Temperature Range

| | |
|--------------|---------------|
| LTC1326C-2.5 | 0°C to 70°C |
| LTC1326I-2.5 | –40°C to 85°C |

Storage Temperature Range –65°C to 150°C

Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

| | | | |
|--|----------------------|--|----------------------------------|
|  <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 160^{\circ}C/W$</p> | ORDER PART NUMBER |  <p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$</p> | ORDER PART NUMBER |
| | LTC1326CMS8-2.5 | | LTC1326CS8-2.5 LTC1326IS8-2.5 |
| | MS8 PART MARKING | | S8 PART MARKING |
| | LTEK | | 132625 326I25 |

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$V_{CC3} = 3.3V$, $V_{CC25} = 2.5V$, $V_{CCA} = V_{CC3}$, $T_A = 25^{\circ}C$ unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------|--|--|---------|-------|-------|---------|
| V_{RT3} | Reset Threshold V_{CC3} | $0^{\circ}C \leq T_A \leq 70^{\circ}C$ | ● 3.094 | 3.118 | 3.143 | V |
| | | $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ | ● 3.052 | 3.118 | 3.143 | V |
| V_{RT25} | Reset Threshold V_{CC25} | $0^{\circ}C \leq T_A \leq 70^{\circ}C$ | ● 2.344 | 2.363 | 2.381 | V |
| | | $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ | ● 2.312 | 2.363 | 2.381 | V |
| V_{RTA} | Reset Threshold V_{CCA} | $0^{\circ}C \leq T_A \leq 70^{\circ}C$ | ● 0.992 | 1.000 | 1.007 | V |
| | | $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ | ● 0.980 | 1.000 | 1.007 | V |
| V_{CC} | V_{CC3} Operating Voltage | \overline{RST} in Correct Logic State | ● 1 | | 7 | V |
| I_{VCC3} | V_{CC3} Supply Current | $\overline{PBR} = V_{CC3}$ | ● | 20 | 40 | μA |
| I_{VCC25} | V_{CC25} Input Current | $V_{CC25} = 2.5V$ | ● | 2.8 | 7 | μA |
| I_{VCCA} | V_{CCA} Input Current | $V_{CCA} = 1V$ | | | | |
| | | $0^{\circ}C \leq T_A \leq 70^{\circ}C$ | ● –5 | 0 | 5 | nA |
| | | $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ | ● –15 | 0 | 15 | nA |
| t_{RST} | Reset Pulse Width | \overline{RST} Low with 10k Ω Pull-Up to V_{CC3} | | | | |
| | | $0^{\circ}C \leq T_A \leq 70^{\circ}C$ | ● 140 | 200 | 280 | ms |
| | | $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ | ● 140 | 200 | 300 | ms |
| t_{SRST} | Soft Reset Pulse Width | \overline{SRST} Low with 10k Ω Pull-Up to V_{CC3} | ● 50 | 100 | 200 | μs |
| t_{UV} | V_{CC} Undervoltage Detect to \overline{RST} | V_{CC25} , V_{CC3} or V_{CCA} Less Than Reset Threshold V_{RT} by More Than 1% | | 13 | | μs |
| I_{PBR} | \overline{PBR} Pull-Up Current | $\overline{PBR} = 0V$ | | | | |
| | | $0^{\circ}C \leq T_A \leq 70^{\circ}C$ | ● 3 | 7 | 10 | μA |
| | | $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ | ● 3 | 7 | 15 | μA |

ELECTRICAL CHARACTERISTICS

$V_{CC3} = 3.3V$, $V_{CC25} = 2.5V$, $V_{CCA} = V_{CC3}$, $T_A = 25^\circ C$ unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------|---|--|------------|------------|------------|--------|
| V_{IL} | \overline{PBR} , \overline{RST} Input Low Voltage | | | | 0.8 | V |
| V_{IH} | \overline{PBR} , \overline{RST} Input High Voltage | | 2 | | | V |
| t_{PW} | \overline{PBR} Min Pulse Width | | 40 | | | ns |
| t_{DB} | \overline{PBR} Debounce | Deassertion of \overline{PBR} Input to \overline{SRST} Output (\overline{PBR} Pulse Width = $1\mu s$) | | 20 | 35 | ms |
| t_{PB} | \overline{PBR} Assertion Time for Transition from Soft to Hard Reset Mode | \overline{PBR} Held Less Than V_{IL} $0^\circ C \leq T_A \leq 70^\circ C$ $-40^\circ C \leq T_A \leq 85^\circ C$ | 1.4 1.4 | 2.0 2.0 | 2.8 3.0 | s s |
| V_{OL} | \overline{RST} Output Voltage Low | $I_{SINK} = 5mA$ | | 0.15 | 0.4 | V |
| | | $I_{SINK} = 100\mu A$, $0^\circ C \leq T_A \leq 70^\circ C$ | | 0.05 | 0.4 | V |
| | | $V_{CC3} = 1V$, $V_{CC25} = 0V$ | | 0.05 | 0.4 | V |
| | | $V_{CC3} = 0V$, $V_{CC25} = 1V$ | | 0.05 | 0.4 | V |
| | | $V_{CC3} = 1V$, $V_{CC25} = 1V$ | | 0.05 | 0.4 | V |
| | | $I_{SINK} = 100\mu A$, $-40^\circ C \leq T_A \leq 85^\circ C$ | | 0.05 | 0.4 | V |
| | | $V_{CC3} = 1.1V$, $V_{CC25} = 0V$ | | 0.05 | 0.4 | V |
| V_{OH} | \overline{SRST} Output Voltage Low | $I_{SINK} = 2.5mA$ | | 0.15 | 0.4 | V |
| | | $I_{SINK} = 2.5mA$ | | 0.15 | 0.4 | V |
| | | $I_{SOURCE} = 1\mu A$ | | | | V |
| | | $I_{SOURCE} = 1\mu A$ | | | | V |
| | \overline{RST} Output Voltage High (Note 3) | $I_{SOURCE} = 1\mu A$ | | | | V |
| | | $I_{SOURCE} = 600\mu A$ | | | | V |
| | | $I_{SOURCE} = 600\mu A$ | | | | V |
| t_{PHL} | Prop Delay \overline{RST} to \overline{RST} High Input to Low Output | $C_{RST} = 20pF$ | | 25 | | ns |
| t_{PLH} | Prop Delay \overline{RST} to \overline{RST} Low Input to High Output | $C_{RST} = 20pF$ | | 45 | | ns |

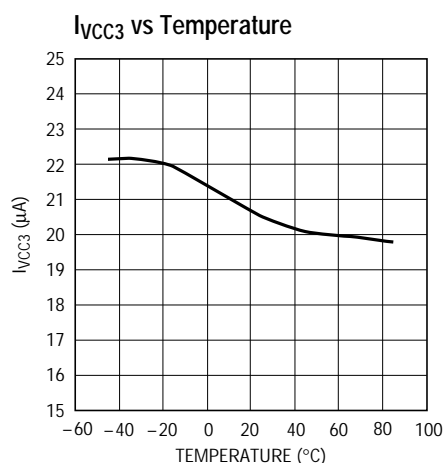
The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

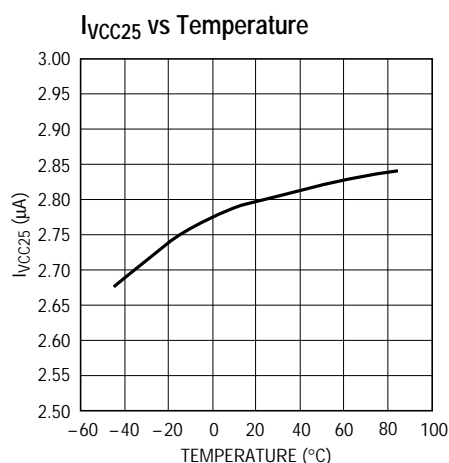
Note 2: All voltage values are with respect to GND.

Note 3: The output pins \overline{SRST} and \overline{RST} have weak internal pull-ups to V_{CC3} of $6\mu A$ typ. However, external pull-up resistors may be used when faster rise times are required.

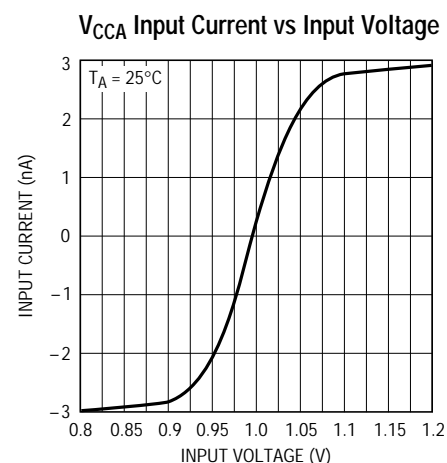
TYPICAL PERFORMANCE CHARACTERISTICS



1326 G01

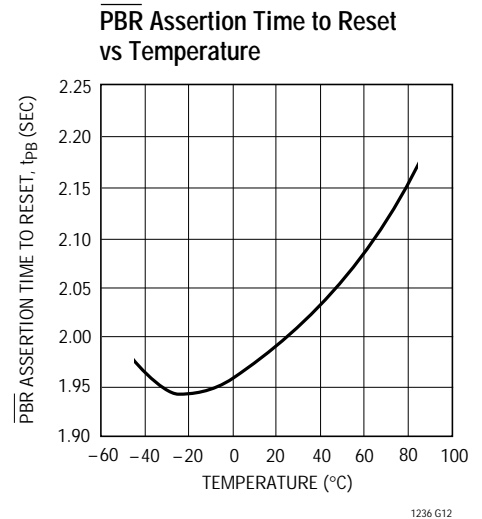
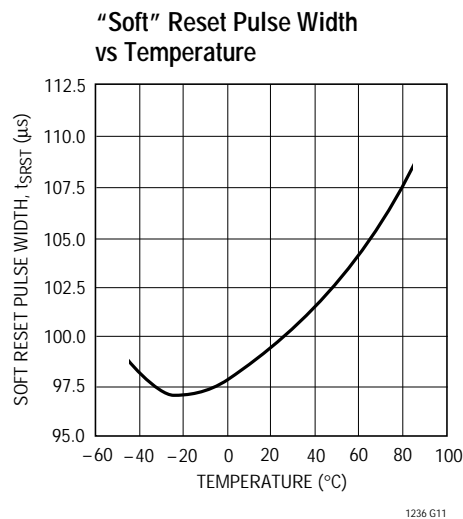
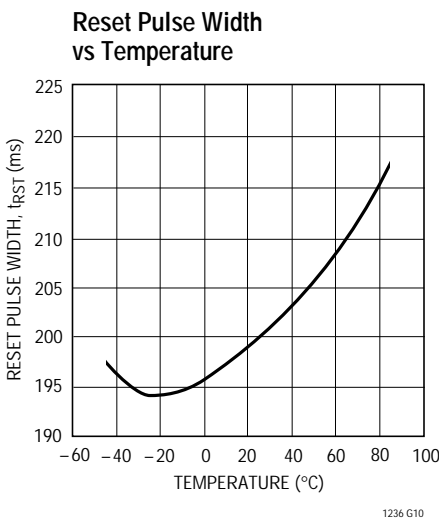
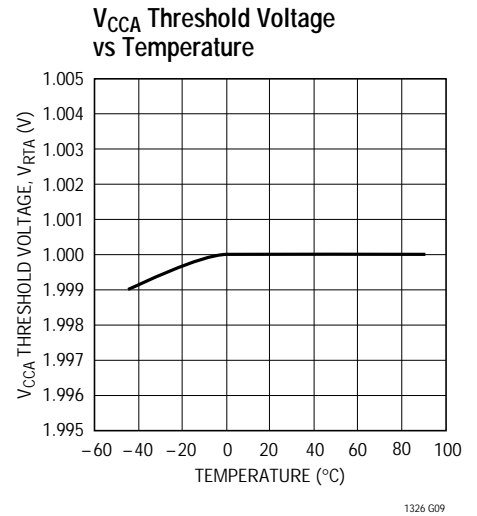
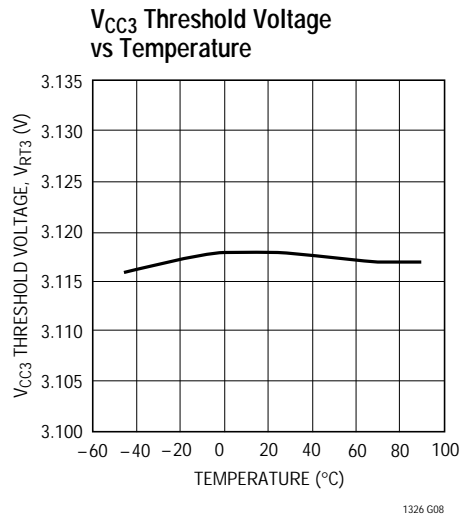
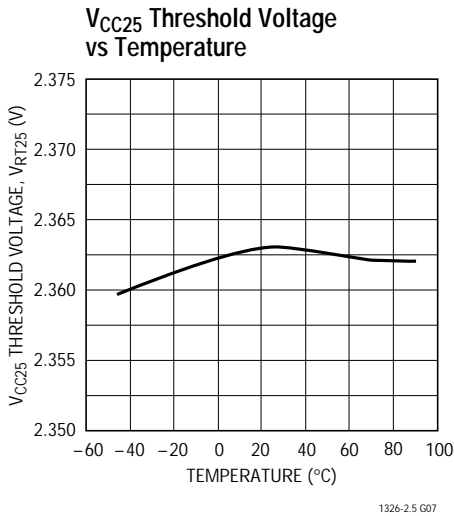
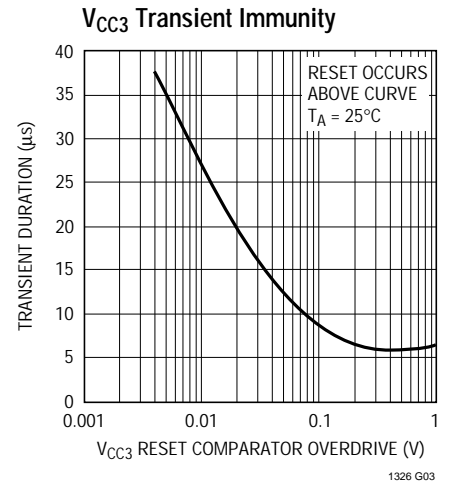
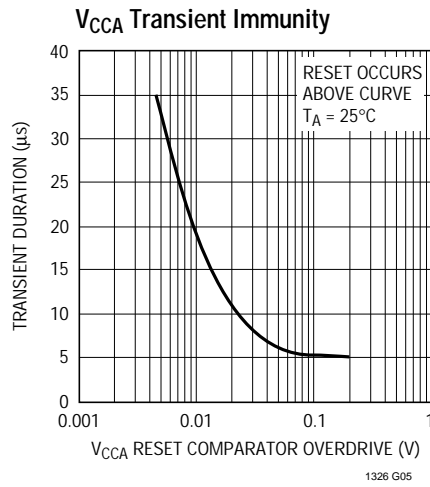
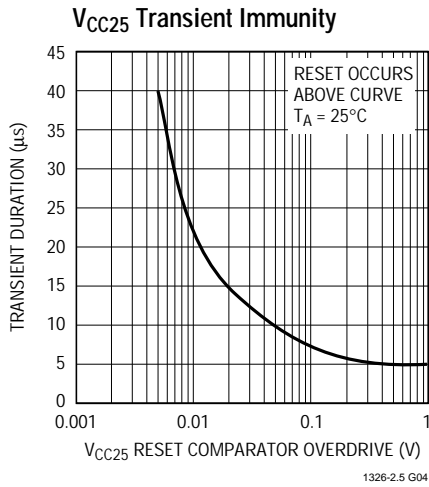


1326-2.5 G02



1326 G06

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

V_{CC3} (Pin 1): 3.3V Sense Input and Power Supply Pin for the IC. Bypass to ground with $\geq 0.1\mu\text{F}$ ceramic capacitor.

V_{CC25} (Pin 2): 2.5V Sense Input. Used as gate drive for RST output FET when the voltage on V_{CC3} is less than the voltage on V_{CC25}. If unused it can be tied to V_{CC3}.

V_{CCA} (Pin 3): 1V Sense, High Impedance Input. Can be used as a logic input with a 1V threshold. If unused it can be tied to either V_{CC3} or V_{CC25}.

GND (Pin 4): Ground.

RST (Pin 5): Reset Logic Output. Active high CMOS logic output, drives high to V_{CC3}, buffered complement of $\overline{\text{RST}}$. An external pull-down on the RST pin will drive this pin high.

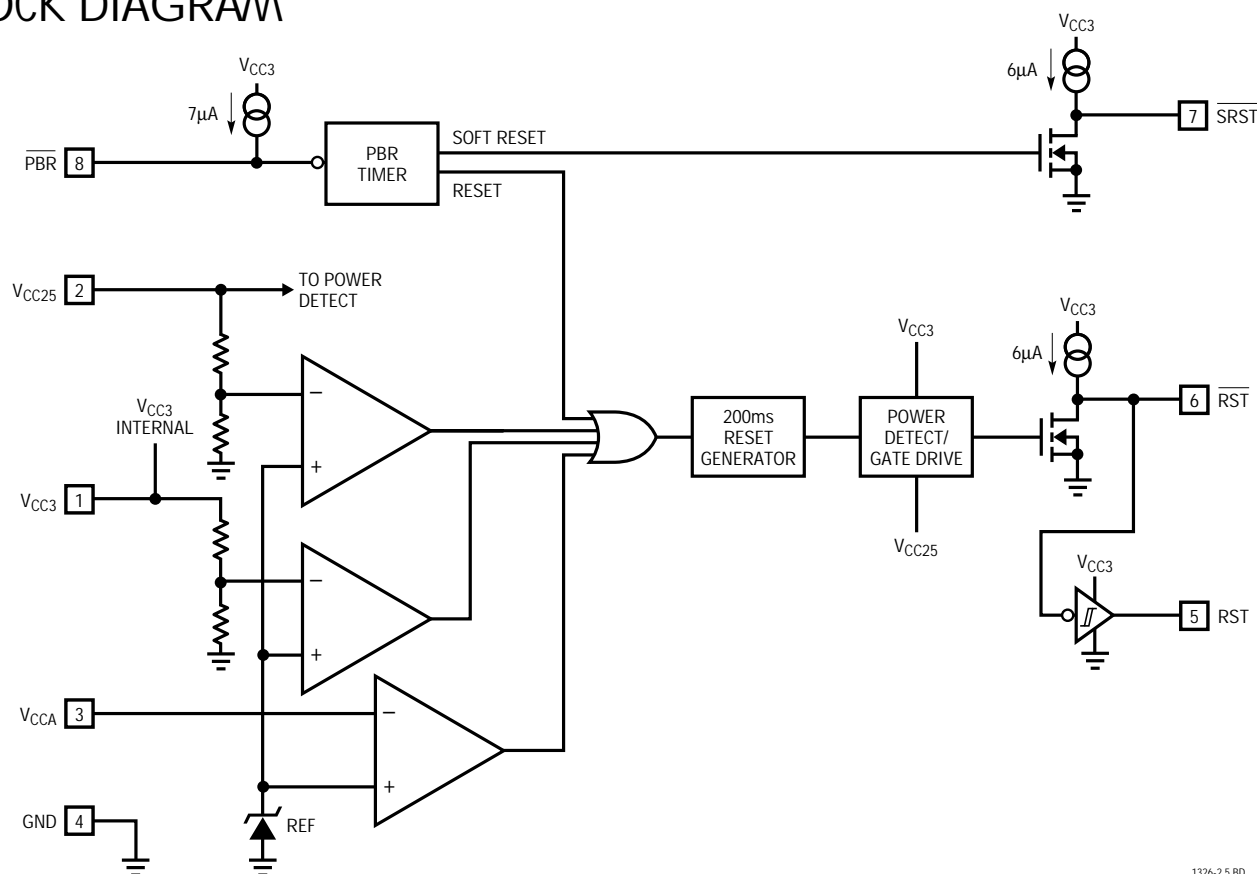
$\overline{\text{RST}}$ (Pin 6): Reset Logic Output. Active low, open-drain logic output with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. Asserted

when one or more of the supplies are below trip thresholds and held for 200ms after all supplies become valid. Also asserted after PBR is held low for more than 2 seconds and for an additional 200ms after PBR is released.

$\overline{\text{SRST}}$ (Pin 7): Soft Reset. Active low, open-drain logic output with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. Asserted for 100 μs after PBR is held low for less than 2 seconds and released.

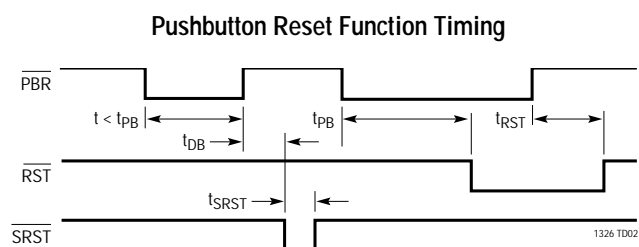
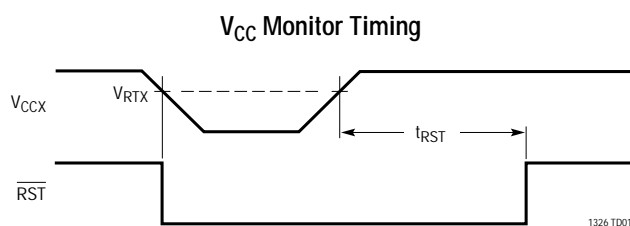
PBR (Pin 8): Pushbutton Reset. Active low logic input with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. When asserted for less than 2 seconds, outputs a soft reset 100 μs pulse on the $\overline{\text{SRST}}$ pin. When PBR is asserted for greater than 2 seconds, the RST output is forced low and remains low until 200ms after PBR is released.

BLOCK DIAGRAM



1326-2.5 BD

TIMING DIAGRAMS



APPLICATIONS INFORMATION

Operation

The LTC1326-2.5 is a micropower, high accuracy triple supply monitoring circuit. The part has two basic functions: generation of a reset when power supplies are out of range, and generation of reset or a “soft” reset when the PBR is pulled low.

Supply Monitoring

All three V_{CC} inputs must be above predetermined thresholds for 200ms before the reset output is released. The LTC1326-2.5 will assert reset during power-up, power-down and brownout conditions on any one or more of the V_{CC} inputs.

On power-up, either the V_{CC25} or V_{CC3} pin can power the drive circuits for the RST pin. This ensures that RST will be low when either V_{CC25} or V_{CC3} reaches 1V. As long as any one of the V_{CC} inputs is below its predetermined threshold, RST will stay a logic low. Once all of the V_{CC} inputs rise above their thresholds, an internal timer is started and RST is released after 200ms. The RST pin outputs the inverted state of what is seen on RST pin.

RST is reasserted whenever any one of the V_{CC} inputs drops below its predetermined threshold and remains asserted until 200ms after all of the V_{CC} inputs are above their thresholds.

On power-down, once any of the V_{CC} inputs drop below its threshold, RST is held at a logic low. A logic low of 0.4V is guaranteed until V_{CC3} and V_{CC25} drop below 1V.

The three precision voltage comparators internal to the LTC1326-2.5 have response times that are typically 13μs. This slow response time helps prevent mistripping due to transients on each of the V_{CC} inputs. The part's ability to suppress transients can be improved by bypassing each of the V_{CC} inputs with a 0.1μF capacitor to ground.

Pushbutton Reset

The LTC1326-2.5 provides a pushbutton reset input pin. The PBR input has an internal pull-up current source to V_{CC3}. If the PBR pin is not used it can be left floating.

When the PBR is pulled low for less than t_{PB} (≈ 2 sec), a narrow (100μs typ) soft reset pulse is generated on the SRST output pin after the button is released. The pushbutton circuitry contains an internal debounce counter which delays the output of the soft reset pulse by typically 20ms. This pin can be OR-tied to the RST pin and issue what is called a “soft” reset. The SRST thereby resets the microprocessor without interrupting the DRAM refresh cycle. In this manner DRAM information remains undisturbed. Alternatively, SRST may be monitored by the processor to initiate a software-controlled reset.

When the PBR pin is held low for longer than t_{PB} (≈ 2 sec), a standard reset is generated. Once the 2 second period has elapsed, a reset signal is produced by the pushbutton logic, thereby clearing the reset counter. Once the button is released, the reset counter begins counting the reset period (200ms nominal). Consequently, the reset outputs remain asserted for approximately 200ms after the button is released.

APPLICATIONS INFORMATION

During a supply induced reset condition, the ability of the PBR pin to force a soft reset condition on the $\overline{\text{SRST}}$ pin is disabled. In other words $\overline{\text{SRST}}$ will remain high. If the PBR pin is held low, both during and after a supply induced reset (low $\overline{\text{RST}}$), the $\overline{\text{RST}}$ pin will remain low until 200ms after the PBR goes high.

3V or 2.5V Power Detect/Gate Drive

The LTC1326-2.5 for the most part is powered internally from the V_{CC3} pin. The exception is at the gate drive of the output FET on the $\overline{\text{RST}}$ pin. On the input to this FET is power detection circuitry used to detect and drive the gate from either the 3.3V input pin (V_{CC3}) or the 2.5V input pin (V_{CC25}). The gate drive is derived from the pin with the highest potential. This ensures the part pulls the $\overline{\text{RST}}$ pin low as soon as either input pin is $\geq 1\text{V}$.

Dual and Single Supply Monitor Operation

The V_{CC3} , V_{CC25} and V_{CCA} inputs may be individually disabled by the following techniques which allows the LTC1326-2.5 to be used as a dual or single supply monitor.

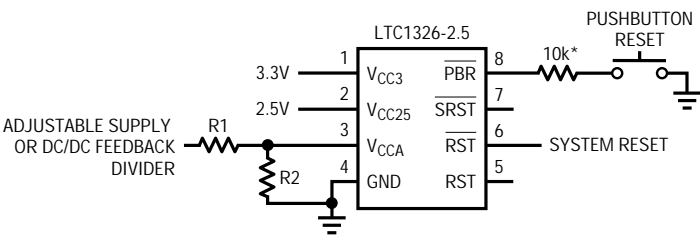
The V_{CCA} pin, if unused, can be tied to either V_{CC3} or V_{CC25} . This is an obvious solution since the trip points for V_{CC3} and V_{CC25} will always be greater than the trip point for V_{CCA} . Likewise, the V_{CC25} , if unused, can be tied to V_{CC3} . V_{CC3} must always be used. Tying V_{CC3} to V_{CC25} and operating off of a 2.5V supply will result in the continuous assertion of $\overline{\text{RST}}$.

Extending ESD Tolerance on the $\overline{\text{PBR}}$ Input Pin

The $\overline{\text{PBR}}$ pin is susceptible to ESD since it can be brought out to a front panel in normal applications. The ESD tolerance of this pin can be increased by adding a resistor in series with the $\overline{\text{PBR}}$ pin. A 10k resistor can increase the ESD tolerance of the $\overline{\text{PBR}}$ pin to approximately 10kV. The $\overline{\text{PBR}}$'s internal pull-up current of 7 μA typical means there is only 70mV (150mV max) dropped across the resistor.

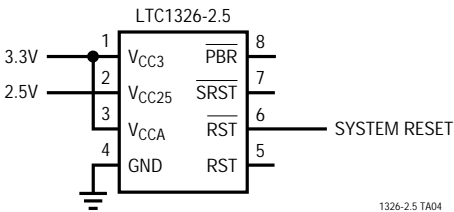
TYPICAL APPLICATIONS

Triple Supply Monitor (3.3V, 2.5V and Adjustable)



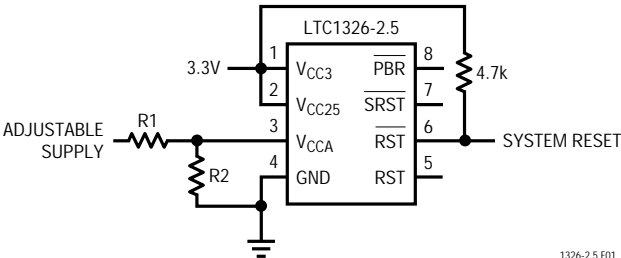
*OPTIONAL RESISTOR EXTENDS ESD TOLERANCE OF $\overline{\text{PBR}}$ INPUT TO APPROXIMATELY 10kV
1326-2.5 TA03

Dual Supply Monitor (3.3V and 2.5V, Deaf V_{CCA} Input)



1326-2.5 TA04

Dual Supply Monitor (3.3V plus Adj)



1326-2.5 F01

LTC1326-2.5

PBR 8

3.3V

4.7k

6 μ A

SRST 7

RESET

6 μ A

RST 6

OTHER OPEN DRAIN
RESET SOURCES
OR-TIED TO RESET

VCC3

RST 5

RESET

1326-2.5 TA05

LTC1435

V_{OSENSE}

6

35.7k 1%

2.8k 1%

22.1k 1%

ADJUSTABLE RESET TRIP THRESHOLD 2.74V

2.9V

3.3V

2.5V

LTC1326-2.5

1 V_{CC3}

2 V_{CC25}

3 V_{CCA}

4 GND

8 PBR

7 SRST

6 RST

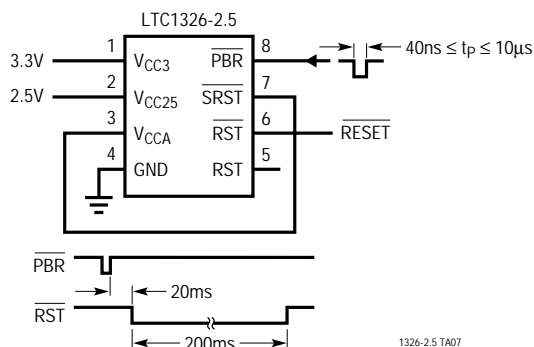
5 RST

SYSTEM RESET

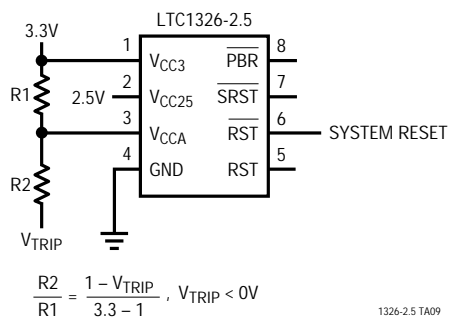
1326-2.5 TA06

TYPICAL APPLICATIONS

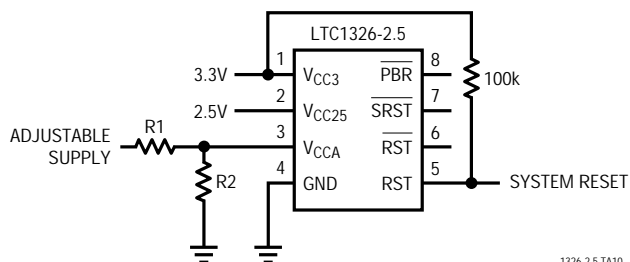
Using the Short Pulse Width, Pushbutton Soft Reset Feature to Initiate Hard Reset



Monitoring a Negative Supply

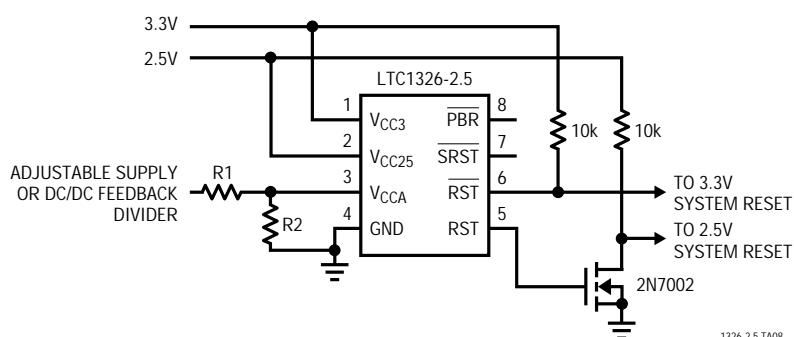


Reset Valid for V_{CC3} Down to 0V



TYPICAL APPLICATION

Triple Supply Monitor with Both 3.3V and 2.5V System Reset Outputs



RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|-------------|--|---|
| LTC690 | 5V Supply Monitor, Watchdog Timer and Battery Backup | 4.65V Threshold |
| LTC694-3.3 | 3.3V Supply Monitor, Watchdog Timer and Battery Backup | 2.9V Threshold |
| LTC699 | 5V Supply Monitor and Watchdog Timer | 4.65V Threshold |
| LTC1232 | 5V Supply Monitor, Watchdog Timer and Pushbutton Reset | 4.37V/4.62V Threshold |
| LTC1326 | Micropower Precision Triple Supply Monitor | 4.725V, 3.118V, 1V Thresholds ($\pm 0.75\%$) |
| LTC1536 | Precision Triple Supply Monitor for PCI Applications | Meets PCI t_{FAIL} Timing Specifications |